Lab 14 - Common-Emitter Amplifier Biasing and Gain

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1/14/22

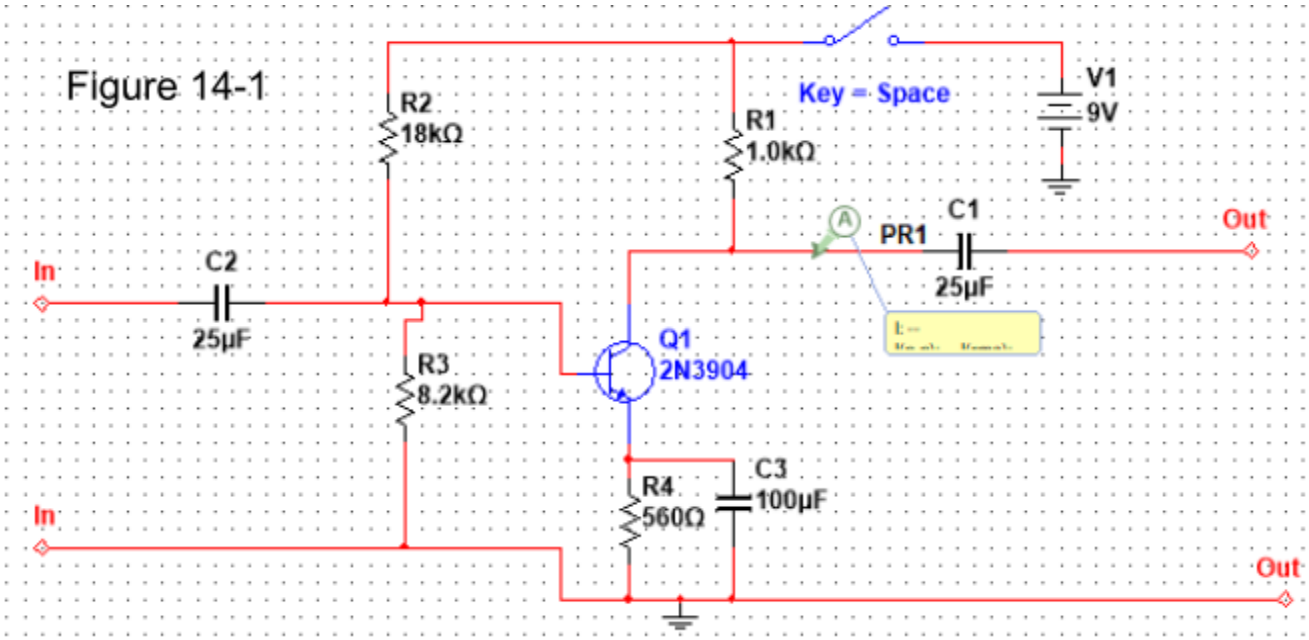
Objectives:

- To connect a transistor as a CE ac amplifier using voltage divider bias
- To measure the voltage gain of a CE amplifier
- To observe the effect of an emitter bypass circuit on amplifier gain

Procedure:

1. We gathered the following materials:
    - A computer
    - Multisim
    - A breadboard
    - Function generator
    - Oscilloscope
    - DC power supply
    - 2N3904 transistor (instead of 2N6004)
    - 22 uF capacitor (2) (Instead of 25uF)
    - 100 uF capacitor
    - 18 kΩ resistor
    - 8.2 kΩ resistor
    - 1 kΩ resistor
    - 560 Ω resistor
    - Wire
    - Digital multimeters (2)

2. We constructed the circuit in figure 14-1 in multisim and on a breadboard



3. We closed the switch in the circuit and measured the current from the collector with the probe in multisim and with the DMM on the breadboard. We recorded this data in table 14-1B for the data on the breadboard, and table 14-1M for the data from Multisim
4. We measured the Base to emitter voltage V_{BE} and recorded it in Tables 14-1M and B
5. We measured the emitter voltage V_E and recorded it in Tables 14-1M and B
6. We measured the collector to emitter voltage V_{CE} and recorded it in Tables 14-1M and B
7. We were able to calculate the emitter current I_E by dividing the voltage found at the emitter V_E by the resistance of resistor R_E. In multisim this was calculated to be equal to 3.55mA and on the breadboard it was equal to 4.02mA
8. We were also able to calculate I_E using the equations from Thevenin's theorem.
9. First, we found the Thevenin voltage using the equation $V_{Th} = \frac{(V_{CC})(R_2)}{R_1+R_2}$. This was found to be 2.82v in both multisim and on the breadboard
10. Next we found the Thevenin resistance using the equation $R_{Th} = \frac{(R_1)(R_2)}{R_1+R_2}$. This was found to be 5,633.6 Ohms on both the breadboard and in Multisim
11. To find the emitter current we used the equation $I_E = \frac{V_{Th}-V_{BE}}{R_E+R_{Th}/\beta}$. Using a beta value of 100, I_E was found to be 3.44mA in multisim, and 3.41mA on the breadboard
12. The difference in current derived from Thevenin's Theorem vs. that derived from Ohm's Law can be explained by the fact that Ohm's law used more experimental values and was subject to imperfect values of resistors and voltage readings.
13. We connected a Signal generator to the "In" connectors of the circuit. The generator was set to 1kHz frequency and 1mV_{RMS}.
14. We connected channel one of our oscilloscope to the output of the circuit and set up the oscilloscope for proper viewing
15. We turned the circuit on and increased the voltage output of the signal generator until the oscilloscope began to show a distorted sine wave. On Multisim this became apparent at a signal voltage of 11 mV. On the breadboard this occurred at 41 mV
16. We lowered the Input voltage just below the point of distortion and recorded the input voltages in Tables 14-1M and 14-1B, We also used the oscilloscope to record the output Peak to peak voltages and record images of the input and output waveforms.
17. We used the digital multimeters in real life and in multisim to record the values of V_{CE}, I_C, and V_{BE} in tables 14-1M, and 14-1B
18. We lowered the Input voltage until the output waveform no longer became consistent with the undistorted output and then raised it so it was slightly above

the minimum distortion and recorded the input voltages in Table 14-1B, We also used the oscilloscope to record the output Peak to peak voltages and record images of the input and output waveforms. This was not possible in multisim because the waveform would never distort when the input signal was lowered

19. We used the digital multimeters in real life and in multisim to record the values of V_{CE}, I_C, and V_{BE} in table 14-1B and 14-1M

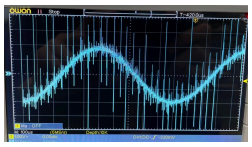
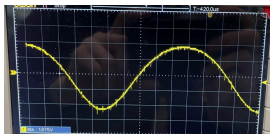
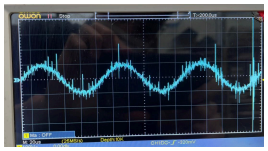
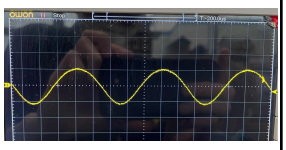
X	X	Voltage V	Voltage V	Voltage V	Waveform	Wave form	Waveform	Wave form
Step	Current mA I_C	V_{BE}	V_{CE}	V_E	Input	mV_{P-P}	Output	V_{P-P}
2	3.62	0.72	2.04	2.25	X	X	X	X
4	3.44	0.71	3.66	1.95		40		4
5	3.44	0.71	3.65	1.98		20		2

Table 14-1B

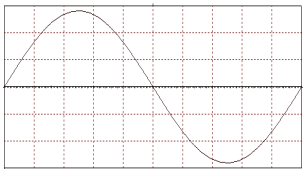
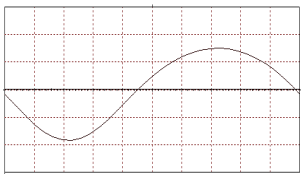
X	X	Voltage V	Voltage V	Voltage V	Waveform	Wave form	Waveform	Wave form
Step	Current mA I_C	V_{BE}	V_{CE}	V_E	Input	mV_{P-P}	Output	V_{P-P}
2	3.53	0.70	3.47	1.99	X	X	X	X
4	3.54	0.70	3.47	1.92		28.28		3.34
5	3.54	0.70	3.47	1.98	X	X	X	X

Table 14-1M

20. We then adjusted the output of the signal generator for half of the maximum undistorted input voltage which was about 14.14mV_{PP} in multisim and 30mV_{PP} in the breadboard

21. We used the oscilloscope and multimeter on multisim and on the breadboard to measure the V_{PP} from each lead of the transistor to ground and record the waveform of these measurements
22. We recorded our data from the breadboard in Table 14-2B and our data from multisim in table 14-2M
23. We then calculated the AC gain of the circuit by dividing the V_{PP} at the collector by the V_{PP} of the base and recorded the gain in Tables 14-2M and 14-2B
24. Next we removed C_3 from the circuit and repeated the process mentioned in steps 21-23 once again recording data in Tables 14-2M and 14-2B
25. Next we placed a short across R_4 in the circuit and repeated the process mentioned in steps 21-23 once again recording data in Tables 14-2M and 14-2B
26. It Can be seen that when R_4 is shorted, the output wave becomes majorly distorted in comparison to the input wave

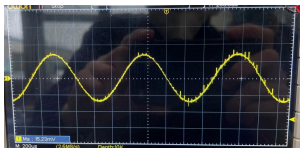
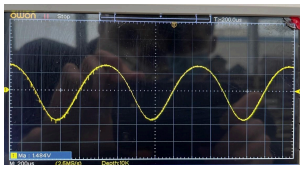
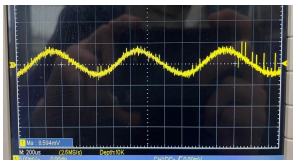
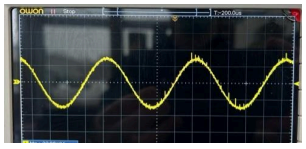
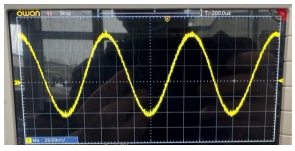
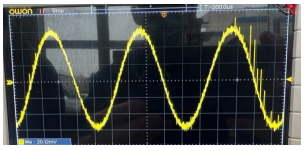
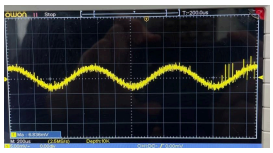
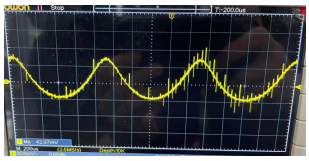
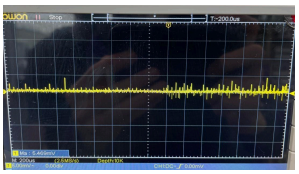
X	Waveform (to Ground)		Waveform (to Ground)		Waveform (to Ground)		X
Step	Base	mV_{P-P}	Collector	mV_{P-P}	Emitter	mV_{P-P}	Gain
7,8		30		3000		5	100
9,10		30		42		30	1.4
11,12		10		45		0	4.5

Table 14-2B

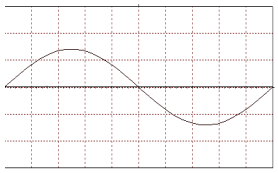
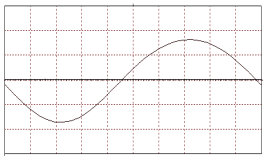
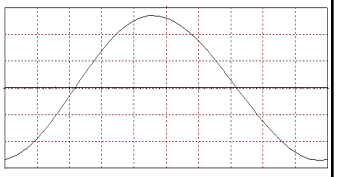
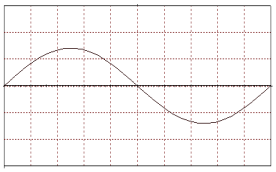
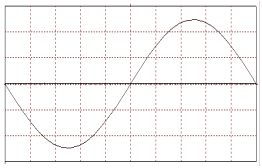
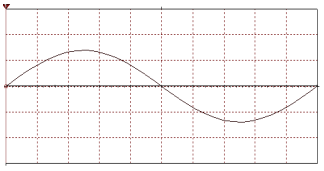
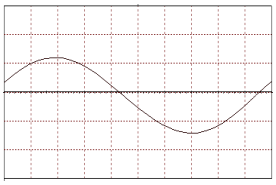
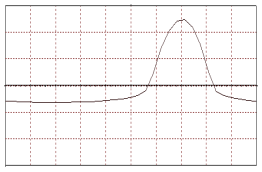
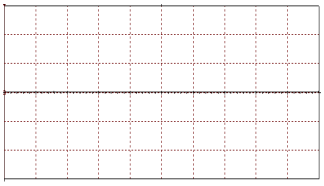
X	Waveform (to Ground)		Waveform (to Ground)		Waveform (to Ground)		X
Step	Base	mV_{P-P}	Collector	mV_{P-P}	Emitter	mV_{P-P}	Gain
7,8		14.14		1700		2.71	120.23
9,10		14.14		24.69		13.92	1.75
11,12		13.22		62.60		0.00	4.736

Table 14-2M

Observations:

1. Q: What is the purpose of C_E in Fig, 14-5? What happens to the ac amplifier gain when it is removed?
   A: Its purpose is to allow the ac to bypass R_E in order to allow much greater amplification for the wave and higher gain. As shown in table 14-2, steps 7,8 show the gain as 120.23 but when it is removed in step 9,10, the gain is much lower at 1.75 which shows that the capacitor is the main reason for a high amplification and gain in this circuit.
2. Q: What is the effect on the amplifier performance of omitting R_E?
   A: When omitting R_E, the amplifier performance decreases as once R_E is removed, the wave becomes more distorted then with the wave with R_E in the circuit. This can be shown in table 14-2 when in step 9,10 the waveform for the collector wasn't distorted and this was with the R_E still in the circuit, but when R_E was removed in step 11,12, the collector wave can be seen as very distorted, decreasing its preformance.

Discussion:

Problem: Our oscilloscope was giving readings contrary to the multisim data

Troubleshooting: we calibrated our oscilloscope and asked our groupmate that did the multisim to help

Solution: We eventually found that our oscilloscope was accidentally set to have the probe on the times 10 setting by our groupmate who set up the oscilloscope.

Conclusion:

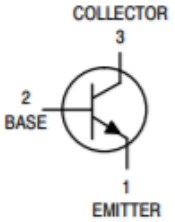
- We connected a transistor as a CE ac amplifier using voltage divider bias in step 2 when we constructed the circuit shown in figure 14-1. We built the circuit so that R2 and R3 act as a voltage divider for the 9 V DC supply and supply a dc voltage to amplify the input waveform using a transistor. The voltage divider also supplies dc to the base or inout in addition to ac which allows the ac to ride on top of the dc so it can pass through the transistor with the emitter base junction remaining in forward bias, resulting in an output waveform with no distortion.
- We calculated the voltage gain of a CE amplifier as shown in table 14-2B where we took the peak-to-peak voltages of the base and collector to get 3 V on the collector (output) and 30 mV on the base (input). We then divided the output voltage of the amplifier (the collector voltage of 3 V) by the input voltage (the base voltage of 30 mV) so that $V_{OUT}/V_{IN}=100$ as the gain.
- We observed the effect of an emitter bypass circuit in table 14-2B when we first took the collector (output) and base (input) voltages (note: all voltages are in peak-to-peak), as well as voltage gain for the circuit with the emitter-bypass circuit. We got values of 30 mV for input voltage and 3 V for output voltage, resulting in a gain of 100. We then removed the capacitor of the emitter-bypass circuit and measured again, getting an input voltage of 30 mV and an output voltage of 42 mV, resulting in a much worse gain of 1.4. Next, we removed the resistor of the emitter-bypass circuit and measured again, getting an input voltage of 10 mV and an output voltage of 45 mV resulting in a slightly better gain of 4.5, but some distortion on the output waveform.

Datasheet:
2N3904:

General Purpose Transistors

NPN Silicon

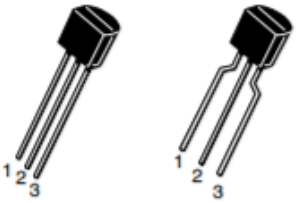
2N3903, 2N3904



Features

- Pb–Free Packages are Available*

TO–92
CASE 29
STYLE 1



MAXIMUM RATINGS

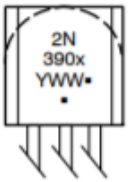
Rating	Symbol	Value	Unit
Collector – Emitter Voltage	V_{CEO}	40	Vdc
Collector – Base Voltage	V_{CBO}	60	Vdc
Emitter – Base Voltage	V_{EBO}	6.0	Vdc
Collector Current – Continuous	I_C	200	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS (Note 1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	83.3	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Indicates Data in addition to JEDEC Requirements.

MARKING DIAGRAMS



x = 3 or 4
Y = Year
WW = Work Week
• = Pb–Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.